SEMESTER S7

HIGH SPEED INTEGRATED CIRCUITS

Course Code	**PEEVT 744**	**CIE Marks**	40
Teaching Hours/Week (L: T:P: R)	3:0:0:0	**ESE Marks**	60
Credits	3	**Exam Hours**	2 Hrs. 30 Min.
Prerequisites (if any)	PCEVT503 VLSI Technology	**Course Type**	Theory

Course Objectives:

1. Understand the fundamental principles of high-speed circuit operation, including signal integrity and the impact of transmission lines on high-speed signals.
2. Develop the ability to design high-speed digital circuits with a focus on clocking, timing analysis, and interconnect design, while optimizing for low power consumption.
3. Gain proficiency in designing high-speed analog components such as amplifiers, comparators, and phase-locked loops, with an emphasis on performance and jitter reduction.
4. Acquire knowledge of advanced design techniques for ensuring signal integrity, high-speed memory design, and the testing and verification of high-speed integrated circuits.

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	Fundamentals of High-Speed Circuit Design Introduction to High-Speed ICs: Importance and applications of high-speed circuits in modern technology, Basic principles of high-speed operation. Signal Integrity: Understanding signal degradation, reflections, and crosstalk, Transmission lines and their impact on signal integrity, Impedance matching and termination techniques. High-Speed CMOS Circuits: Overview of CMOS technology for high-speed applications, Speed-power trade-offs and optimizing performance.	**9**

2	High-Speed Digital Design Techniques Clocking and Timing Analysis: Clock distribution networks and clock skew, Setup and hold times, timing margins. Jitter and its impact on timing accuracy. Interconnect Design: On-chip interconnects: RLC effects and delay modelling, Crosstalk minimization and signal buffering, Advanced interconnects: Optical and 3D interconnects. Low-Power High-Speed Design: Techniques for reducing power consumption in high-speed circuits, Voltage scaling, dynamic voltage, and frequency scaling (DVFS), Power gating and multi-Vt techniques.	**9**
3	High-Speed Analog Design High-Speed Amplifiers and Comparators: Design of wideband amplifiers: Gain-bandwidth trade-offs, Current-mode logic (CML) circuits for high-speed applications, Comparator design and optimization for speed. Phase-Locked Loops (PLL) and Clock Recovery Circuits: Basics of PLLs, Operation and applications, Design of PLL components: VCO, frequency dividers, phase detectors. Techniques for jitter reduction in PLLs. High-Speed Data Converters: Overview of ADCs and DACs in high-speed applications, Design challenges in high-speed data conversion, Techniques for enhancing the performance of data converters.	**9**
4	Module 4: Advanced Topics in High-Speed IC Design Design for Signal Integrity: Techniques for mitigating signal integrity issues, ESD protection and layout considerations for high-speed ICs, Packaging and PCB considerations in high-speed design. High-Speed Memory Design: SRAM, DRAM, and non-volatile memory technologies for high-speed applications, Memory interface design and timing considerations, Emerging memory technologies: MRAM, RRAM, etc. Testing and Verification of High-Speed Circuits: Techniques for testing high-speed digital and analog circuits, Signal integrity testing, eye diagrams, and bit error rate (BER) testing, Design for testability (DFT) and built-in self-test (BIST) methods.	**9**

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination-1 (Written)	Internal Examination-2 (Written)	Total
5	15	10	10	40

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	understand signal integrity issues in high-speed circuits and apply concepts of transmission lines and impedance matching effectively.	**K2**
CO2	design and optimize high-speed digital circuits, considering timing constraints, power consumption, and interconnect challenges.	**K3**
CO3	design high-speed analog components, such as amplifiers and PLLs, with a focus on achieving high performance and minimizing jitter.	**K3**
CO4	apply advanced techniques for ensuring signal integrity, designing high-speed memory systems, and performing thorough testing and verification of high-speed ICs.	**K3**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	1	1	1				1	1	
CO2	2	2	2	1	2	1				1	1	1
CO3	2	2	2	1	2	1				2	1	1
CO4	2	3	3	2	1	1				2	1	2

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages	Brian Young	Prentice Hall Modern Semiconductor Design	2000
2	Design of High-Performance Microprocessor Circuits	Anantha Chandrakasan, William J. Bowhill, Frank Fox	Wiley-IEEE Press	2000
3	High Speed Digital Design: A Handbook of Black Magic	Howard Johnson, Martin Graham	Prentice Hall Modern Semiconductor Design	1993
4	CMOS: Circuit Design, Layout, and Simulation	R. Jacob Baker	IEEE Press Series on Microelectronic Systems	2019

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	High-Speed Signaling: Jitter Modeling, Analysis, and Budgeting	Kyung Suk Oh, Xingchao Yuan	Prentice Hall Modern Semiconductor Design Series	2011
2	Signal Integrity and Radiated Emission of High-Speed Digital Systems	Spartaco Caniggia, Francescaromana Maradei	Wiley	2008
3	Advanced Signal Integrity for High-Speed Digital Designs	Stephen H. Hall, Howard L. Heck	Wiley	2008
4	High-Speed Circuit Board Signal Integrity	Stephen C Thierauf	Artech House	2017

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://nptel.ac.in/courses/108105375
2	https://onlinecourses.nptel.ac.in/noc24_ee134/preview
3	https://archive.nptel.ac.in/courses/117/106/117106030/
4	https://nptel.ac.in/courses/106103016

SEMESTER 7

EMBEDDED NETWORKS

Course Code	PEEVT 746	CIE Marks	40
Teaching Hours/Week (L: T:P: R)	3:0: 0:0	ESE Marks	60
Credits	3	Exam Hours	2 Hrs. 30 Min.
Prerequisites (if any)	PBEVT 504	Course Type	Theory

Course Objectives:

1. To understand Basic Network Architectures and familiarize with network protocols

SYLLABUS

Module No.	Syllabus Description	Contact Hours
1	**Distributed Embedded System**- Basic Network Architectures: Client-Server, Peer-to-Peer, Network Topologies**,** Basic concepts and definitions of LAN, WLAN, WAN &WPAN. OSI and ISO Models in Distributed Embedded Systems**.** Challenges in Designing Distributed Embedded Systems. Examples and applications of distributed embedded systems. **Embedded network protocol** CAN- CAN identifier, different layers, bit encoding, message format, Bus length, baud rate, Arbitration mechanism, Error control, Controller Architecture, Applications, and examples.	7
2	**Ethernet protocol**: Networking Devices-Routers, switches, hubs, and bridges, Ethernet protocol- Features, Frames, MAC, CSMA/CD -Principle, Back-off mechanisms. **Internet protocol**- Higher level protocols -TCP and UDP, IP packet structure- IPv4 and IPv6, Wireless LAN Configurations -Single-cell and multicell, Infrastructure and AdHoc mode, IEEE 802.11 MAC protocol.	10

	Nomadic Access- IEEE 802.11k. **Bluetooth Protocol**: Bluetooth Architecture, Bluetooth network topologies -Piconet and Scatternet. Bluetooth WPAN protocols- LMP and L2CAP, Bluetooth packet format-Classic packet & BLE format. Polling mechanism, Establishing a connection, Power saving modes, Bluetooth applications, Overview of Mobile Ad hoc networks (MANETs) & Vehicular Ad Hoc Networks (VANETs).	
3	**Sensor networking**: Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing. **Operating system basics: Functions** of OS, Kernel, types of operating systems. Introduction to Real-time operating systems: Tasks, process, threads, multiprocessing and multitasking, task scheduling, task communication.	**7**
4	**Introduction to IoT and IoT networking:** devices vs. computers, technical building blocks, Basics of IoT networking, M2M area network, Modbus, ZigBee-Zigbee Architecture- LoRaWAN -Standardization and Alliances. **Introduction to cloud computing**: Data Collection, storage, and computing using a Cloud Platform (Basics Only).	**7**

Course Assessment Method
(CIE: 40 marks, ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

Attendance	Assignment/ Microproject	Internal Examination- 1 (Written)	Internal Examination- 2 (Written)	Total
5	**15**	**10**	**10**	**40**

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

Part A	Part B	Total
• 2 Questions from each module. • Total of 8 Questions, each carrying 3 marks **(8x3 =24marks)**	• Each question carries 9 marks. • Two questions will be given from each module, out of which 1 question should be answered. • Each question can have a maximum of 3 sub-divisions. **(4x9 = 36 marks)**	**60**

Course Outcomes (COs)

At the end of the course, students should be able to:

Course Outcome		Bloom's Knowledge Level (KL)
CO1	Understand basic distributed embedded systems architectures, topologies, and protocols.	**K2**
CO2	Understand the architectures, and principles of operation of ethernet, IP, and Bluetooth.	**K2**
CO3	Understand the concepts of sensor networking and RTOS	**K2**
CO4	Comprehend the concepts of IOT networking and cloud computing	**K2**

Note*: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create*

CO-PO Mapping Table (Mapping of Course Outcomes to Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	**3**		**3**	**3**								**2**
CO2	**3**	**2**	**3**	**3**								**2**
CO3	**3**		**3**	**3**								**2**
CO4	**3**	**2**	**3**	**3**								**2**

Note: *1: Slight (Low), 2: Moderate (Medium), 3: Substantial (High), -: No Correlation*

Text Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Systems Design: A Unified Hardware/Software Introduction.	Frank Vahid, Tony Givargis	John & Wiley Publications	2002
2	"Protocols and Architectures for Wireless Sensor Networks"	Holger Karl and Andreas Wiilig	John Wiley & Sons Limited 2008	2008
3	Operating systems Concepts	Abraham Silber Chatz, Peter Baer Galvin, Greg Gagne	Wiley Publications	
4	Internet of Things -Architectures and Design Principles	Raj Kamal	MacGraw Hill India Private Limited	

Reference Books				
Sl. No	**Title of the Book**	**Name of the Author/s**	**Name of the Publisher**	**Edition and Year**
1	Embedded Ethernet and Internet Complete	Jan Axelson	Penram Publications, 2003.	2003
2	"A Survey on Sensor Networks",	I.F. Akyildiz and Weillian	IEEE Communication Magazine	Aug 2007
3	Embedded systems an integrated approach	Lyla B Das	pearson	Ist edn
3	IoT fundamentals- networking technologies, protocol, and use cases.	David Hanes, Gonzalo Salgueiro et al.	Cisco Press	2017
4	Computers as Components: Principles of Embedded Computing System Design.	Wayne Wolf	Morgan Kaufman Publishers - Elsevier	3ed 2008

Video Links (NPTEL, SWAYAM…)	
Module No.	**Link ID**
1	https://archive.nptel.ac.in/courses/106/105/106105193/
2	https://nptel.ac.in/courses/108105057
3	https://onlinecourses.nptel.ac.in/noc24_cs24/preview
4	https://youtube.com/playlist?list=PLDD18E950D85E018C&si=6wnLOHy0GarETWi1